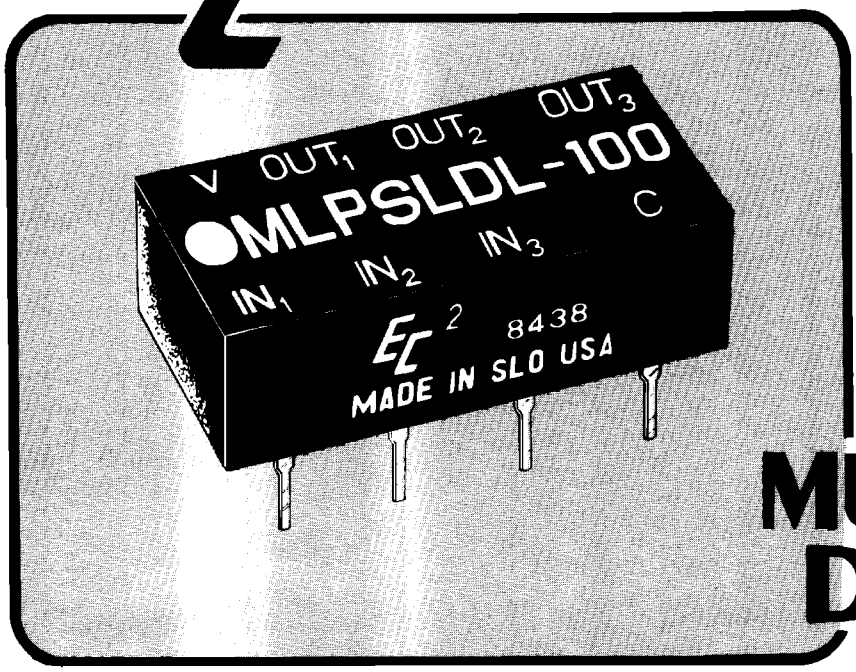
EC²



low profile

T²L COMPATIBLE MULTI-LOGIC DELAY LINE

(LOW POWER SCHOTTKY)

- T²L input and outputs
- Delays stable and precise
- 14-pin DIP package (.250 high)
- Available in delays from 10 to 100ns — each isolated and with 20 low power Schottky fan-out capacity
- Rise time 8ns maximum

design notes

The "DIP Series" Multiple Low Power Schottky Logic Delay Lines developed by Engineered Components Company have been designed to provide precise delays with required driving and pick-off circuitry contained in a single 14-pin DIP package. These logic delay lines are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 1.5 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The MLPSLDL is offered in 31 delays from 10 to 100ns. Each module includes three (3) separate delay lines, each isolated and fully buffered. Delay tolerances are maintained, as shown in the accompanying Part Number Table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.3V level on the leading edge. Rise time for all modules is 8ns maximum, when measured from 0.8V to 2.0V. Temperature coefficient of delay is approximately +1200 ppm/°C over the operating temperature range of 0 to 70°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the output without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each individual delay line has the capability of driving up to 20 low power Schottky loads.

These "DIP Series" modules are packaged in a 14-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive stand off from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

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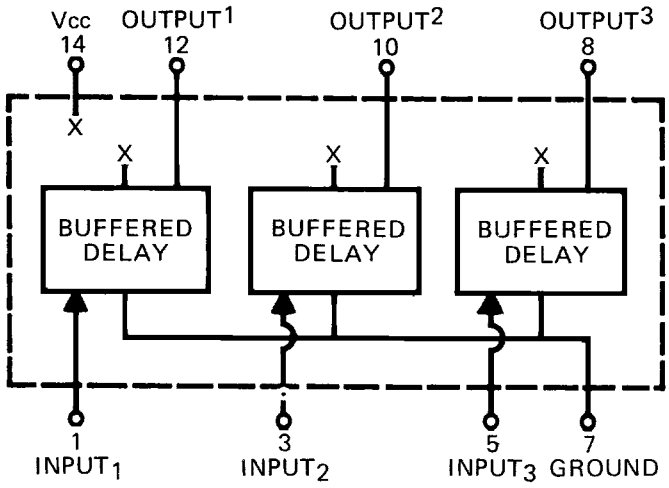
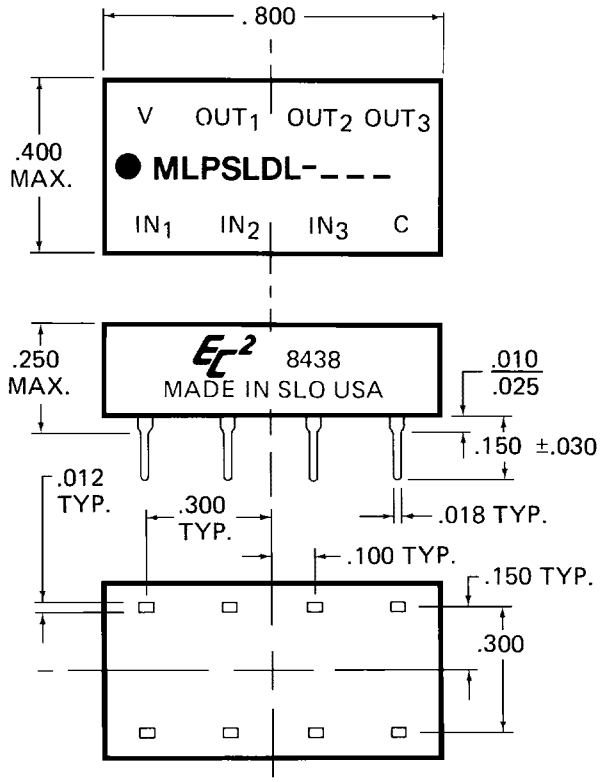
DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC²), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vcc supply voltage is maintained at 5.0V DC.
3. All units are tested using a low power Schottky toggle-type positive input pulse and one low power Schottky T²L load at the output.
4. ϕ Input pulse width used is 100% longer than delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

* Vcc supply voltage:	4.75 to 5.25V DC
Vcc supply current:	
Constant "0" in	16ma typical
Constant "1" in	3ma typical
Logic 1 input:	
Voltage	2V min.; 5.5V max.
Current	2.4V = 20ua max. 5.5V = .1ma max.
Logic 0 input:	
Voltage	.8V max.
Current	–.4ma max. (@.4V in)
Logic 1 Voltage out:	2.7V min.
Logic 0 Voltage out:	.5V max.
Operating temperature range:	0 to 70°C.
Storage temperature:	–55 to +125°C.

* Delays increase or decrease approximately 4% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)			
PART NO.	OUTPUT	PART NO.	OUTPUT
MLPSLDL-10	10 ±1	MLPSLDL-30	30 ±1.5
MLPSLDL-11	11 ±1	MLPSLDL-35	35 ±1.5
MLPSLDL-12	12 ±1	MLPSLDL-40	40 ±1.5
MLPSLDL-13	13 ±1	MLPSLDL-45	45 ±2
MLPSLDL-14	14 ±1	MLPSLDL-50	50 ±2
MLPSLDL-15	15 ±1	MLPSLDL-55	55 ±2
MLPSLDL-16	16 ±1	MLPSLDL-60	60 ±2
MLPSLDL-17	17 ±1	MLPSLDL-65	65 ±2.5
MLPSLDL-18	18 ±1	MLPSLDL-70	70 ±2.5
MLPSLDL-19	19 ±1	MLPSLDL-75	75 ±2.5
MLPSLDL-20	20 ±1	MLPSLDL-80	80 ±2.5
MLPSLDL-21	21 ±1	MLPSLDL-85	85 ±3
MLPSLDL-22	22 ±1	MLPSLDL-90	90 ±3
MLPSLDL-23	23 ±1	MLPSLDL-95	95 ±3
MLPSLDL-24	24 ±1	MLPSLDL-100	100 ±3
MLPSLDL-25	25 ±1		

ϕ All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.